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**AMENDMENT TO THE CLAIMS**

Please replace the currently pending claims with the following:

1. (Currently Amended) A thin-film transistor array of pixels comprising:
  - a first thin-film transistor including a channel, the channel defined by a region between a first electrode and a second electrode, the channel having a defined length and width;
  - a gate line coupled to a gate electrode of the first thin film transistor;
  - a first data line coupled to a source electrode of the first thin film transistor;
  - a drain electrode of the thin-film transistor directly coupled to the display or sensing media;
  - a pixel addressed by the first thin-film transistor, the pixel having two pixel dimensions including a pixel width and a pixel length, the channel width longer than the shorter of the two pixel dimensions.
2. (Original) The thin-film transistor array of claim 1 wherein the ratio of the channel width to the channel length exceeds 5.
3. (Original) The thin film transistor array of claim 1 wherein the pixel width is equal to the pixel length.
4. (Original) The thin film transistor array of claim 1 wherein the channel includes at least one bend.
5. (Original) The thin film transistor array of claim 1 wherein the channel includes at least two bends such that a section of an electrode is surrounded on three sides by the channel in a U configuration.

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6. (Withdrawn) The thin film transistor array of claim 1 wherein the channel completely surrounds one electrode.

7. (Currently Amended) The thin-film transistor array of claim 1 wherein ~~the~~ a semiconductor used in the first thin-film transistor is an organic semiconductor.

8. (Currently Amended) The thin-film transistor array of claim 1 wherein ~~the~~ a semiconductor used in the first thin-film transistor is a polymeric semiconductor.

9. (Withdrawn) The thin-film transistor array of claim 1 wherein the semiconductor is a continuous film over the array.

10. (Original) The thin film transistor array of claim 5 wherein the electrode is the drain electrode.

11. (Original) The thin-film transistor array of claim 1 wherein the pixel is backlit liquid crystal material.

12. (Currently Amended) The thin-film transistor array of claim 1 further comprising:

~~a gate line coupled to a gate electrode of the first thin film transistor; and,~~  
a second thin film transistor including a corresponding gate electrode coupled to the gate line.

13. (Original) The thin film transistor array of claim 1 wherein the channel surrounds a drain electrode.

14. (Original) The thin film transistor array of claim 1 wherein the channel includes a first side and a second side, the first side of the channel coupled to the first electrode, the second side of the channel coupled to the second electrode.

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15. (Original) The thin film transistor array of claim 1 wherein the first electrode is a drain and the second electrode is a source.

16. (Original) The thin film transistor of claim 14 wherein the channel includes a top surface, the top surface couples to a third electrode.

17. (Original) The thin film transistor of claim 16 wherein the third electrode is a gate.

18. (Withdrawn) The thin-film transistor array of claim 1 wherein the channel completely surrounds a source electrode.

19. (Cancelled)

20. (Currently Amended) The thin-film transistor array of claim ~~19~~ 1 further comprising:

a second thin film transistor to address a second pixel, the first data line coupled to a source electrode of the second thin film transistor.

21. (Original) The thin film transistor array of claim 20 further comprising:

a second pixel addressed by the second thin film transistor, the second pixel having two dimensions including a second pixel length and a second pixel width, a channel width of the second thin film transistor greater than the smallest dimension of the second pixel.

22. (Previously Presented) The thin-film transistor array of claim 1 wherein the mobility of a semiconductor used to form the thin film transistor is below  $0.5 \text{ cm}^2/\text{Volt} \cdot \text{second}$ .

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23. (Currently Amended) The thin-film transistor array of claim 1 further comprising:

~~a first gate line coupled to a gate electrode of the first thin film transistor;~~  
a second gate line coupled to a gate of a second thin-film transistor, the second-thin film transistor coupled to a second pixel; and,  
a third gate line coupled to a gate electrode of a third thin-film transistor, the third-thin film transistor coupled to a third pixel.

24. (Original) The thin-film transistor array of claim 23 further comprising:  
a drive circuit coupled to corresponding gate lines of each thin-film transistor, the drive circuit to switch each thin-film transistor to create a pattern in a display.

25. (Original) The thin-film transistor array of claim 23 further comprising:  
a sensing circuit coupled to each gate line to sense the output of each thin-film transistor in a sensor system.

26. (Original) The thin film transistor array of claim 1 wherein the channel width to length ratio exceeds 50.

27 – 32 (Cancelled)

32. (New) The thin film transistor array of pixels of claim 1 further comprising:  
an encapsulation layer deposited between a media layer and the drain electrode, vias etched in the encapsulation layer couple the media layer to the drain electrode.